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Logic Synthesis for Field-Programmable Gate Arrays (The Springer International Series in Engineering and Computer Science)

Rajeev Murgai, Robert K. Brayton, Alberto Sangiovanni-Vincentelli

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Short turnaround has become critical in the design of electronic systems. Software- programmable components such as microprocessors and digital signal processors have been used extensively in such systems since they allow rapid design revisions. However, the inherent performance limitations of software-programmable systems mean that they are inadequate for high-performance designs. Designers thus turned to gate arrays as a solution. User-programmable gate arrays (field-programmable gate arrays, FPGAs) have recently emerged and are changing the way electronic systems are designed and implemented. The growing complexity of the logic circuits that can be packed onto an FPGA chip means that it has become important to have automatic synthesis tools that implement logic functions on these architectures. *Logic Synthesis for Field-Programmable Gate Arrays* describes logic synthesis for both look-up table (LUT) and multiplexor-based architectures, with a balanced presentation of existing techniques together with algorithms and the system developed by the authors.
Audience: A useful reference for VLSI designers, developers of computer-aided design tools, and anyone involved in or with FPGAs.

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